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10/714,216	11/14/2003	Mallinath Hatti	15270US01	2560

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EXAMINER
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PIZIALI, JEFFREY J

ART UNIT	PAPER NUMBER
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2629

MAIL DATE	DELIVERY MODE
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PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/714,216	<b>Applicant(s)</b> HATTI ET AL.	
	<b>Examiner</b> JEFF PIZIALI	<b>Art Unit</b> 2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 30 April 2009.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 8,9,11-14 and 21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 8,9,11-14 and 21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 November 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on *30 April 2009* has been entered.

### *Drawings*

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: " $L_0, L_1, \dots L_x L_{x+1}, L_N$ " (see Fig. 1); "*Video Signal Encoder 55*" (see Fig. 3); and "*835a-835f*" (see Fig. 5).

Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. The drawings have not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the figures.

### ***Specification***

4. The disclosure is objected to because of the following informalities:

The term "***means of a vertical synchronization pulses***" should be corrected (*page 1, paragraph 4, line 5*).

Appropriate correction is required.

5. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### ***Claim Objections***

6. Claim 21 is objected to because of the following informalities:

The term "***the controller does provides***" should be corrected (*line 2*).

Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 8, 9, 11-14, and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Claim 8 recites the limitation "***the display engine***" (*line 5*). There is insufficient antecedent basis for this limitation in the claim.

10. Claim 12 recites the limitation "***the information regarding the first frame***" (*lines 2-3*). There is insufficient antecedent basis for this limitation in the claim.

11. Claim 13 recites the limitation "***the information regarding the first frame***" (*lines 2-3*). There is insufficient antecedent basis for this limitation in the claim.

12. Claim 14 recites the limitation "***the information regarding the first frame***" (*line 2*). There is insufficient antecedent basis for this limitation in the claim.

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13. Claim 21 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***a first horizontal synchronization pulse***" (claim 21, line 4) and "***a first horizontal synchronization pulse***" (claim 8, lines 9-10).

It would be unclear to one having ordinary skill in the art whether these limitations are intended to be identical to, or distinct from, one another.

Another omitted structural cooperative relationship results from the claimed subject matter: "***a vertical synchronization pulse***" (claim 21, lines 4-5) and "***a vertical synchronization pulse***" (claim 8, line 10).

It would be unclear to one having ordinary skill in the art whether these limitations are intended to be identical to, or distinct from, one another.

14. The remaining claims are rejected under 35 U.S.C. 112, second paragraph, as being dependent upon rejected base claims.

15. The claims are rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

As a courtesy to the Applicant, the examiner has attempted to also make rejections over prior art -- based on the examiner's best guess interpretations of the invention that the Applicant is intending to claim.

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However, the indefinite nature of the claimed subject matter naturally hinders the Office's ability to search and examine the application.

Any instantly distinguishing features and subject matter that the Applicant considers to be absent from the cited prior art is more than likely a result of the indefinite nature of the claims.

The Applicant is respectfully requested to correct the indefinite nature of the claims, which should going forward result in a more precise search and examination.

***Claim Rejections - 35 USC § 102 / 103***

16. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

17. Claims 8, 9, 11-14, and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by ***Sotheran (US 5,603,012 A)***.

Regarding claim 8, ***Sotheran*** discloses a system for displaying frames, said system comprising:

a rasterizing circuit [*e.g., 3-buffer system, READY buffer*] for rasterizing [*e.g., converts picture/image data into pixels*] a first frame [*e.g., a first, previous frame of picture data*] (*see the entire document, including Column 325, Lines 55-61*);

a controller [*e.g., buffer manager*] for providing information [*e.g., status information -- e.g., buffer flagged as READY*] regarding a second frame [*e.g., a second, next, new frame of*

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*picture data following the first frame of picture data]* to the rasterizing circuit, after the display engine provides the first frame; and wherein

the rasterizing circuit rasterizes the first frame [*e.g., previous displayed buffer frame picture is repeated*], if the controller does not provide the information [*e.g., buffer not flagged as READY*] regarding the second frame to the rasterizing circuit before a first horizontal synchronization pulse [*e.g., hsync*] following a vertical synchronization pulse [*e.g., vsync*] associated with the second frame (*see the entire document, including Column 295, Line 45 - Column 296, Line 40*).

Sotheran explains, "*The display address generator requests a new display buffer, once every vsync, via a two-wire interface. If there is a buffer flagged as READY, then that will be allocated to display by the buffer manager. If there is no READY buffer, the previously displayed buffer will be repeated*" (see Column 296, Lines 17-21).

Therefore, Sotheran teaches not providing the information [*e.g., buffer not flagged as READY*] regarding the second frame to the display engine following a vertical synchronization pulse [*e.g., wherein vsync for the first frame and second frame are both "associated" -- in different ways -- with the second frame*].

Sotheran also goes on to define 'vdelay' as "*The number of hsync pulses following a vsync pulse before the first line of video or border... The minimum vdelay is zero. The first hsync is the first active line*" (see Column 333, Lines 48-59).

Therefore, Sotheran clearly teaches at least one first horizontal synchronization pulse [*e.g., hsync*] following a vertical synchronization pulse [*e.g., vsync*].



Regarding claim 9, **Sotheran** discloses the rasterizing circuit rasterizes the second frame [e.g., *READY buffer*] if the controller provides the information regarding the second frame before the first horizontal synchronization pulse following the vertical synchronization pulse associated with the second frame (*see the entire document, including Column 295, Line 45 - Column 296, Line 40*).

Regarding claim 11, **Sotheran** discloses a frame buffer [e.g., *three buffers*] for storing the second frame beginning at at least one starting address; and wherein

the information regarding the second frame comprises the at least one starting address (*see the entire document, including Column 295, Line 45 - Column 296, Line 40*).

Regarding claim 12, **Sotheran** discloses a first at least one register [e.g., *three buffers*] for storing the information regarding the first frame (*see the entire document, including Column 295, Line 45 - Column 296, Line 40*).

Regarding claim 13, **Sotheran** discloses the rasterizing circuit rasterizes the first frame based on the information regarding the first frame if the controller does not provide the information regarding the second frame before the the first horizontal synchronization pulse following the vertical synchronization pulse associated with the second frame (*see the entire document, including Column 295, Line 45 - Column 296, Line 40*).

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Regarding claim 14, **Sotheran** discloses the controller overwrites [e.g., *EMPTY buffer*] the information regarding the first frame with the information regarding the second frame and wherein the rasterizing circuit rasterizes the second frame based on the information regarding the second frame (*see the entire document, including Column 295, Line 45 - Column 296, Line 40*).

Regarding claim 21, **Sotheran** discloses the rasterizing circuit rasterizes the second frame, if the controller does provides the information regarding the second frame to the rasterizing circuit after the vertical synchronization pulse associated with the second frame and before a first horizontal synchronization pulse following a vertical synchronization pulse associated with the second frame (*see the entire document, including Column 295, Line 45 - Column 296, Line 40*).

### ***Response to Arguments***

18. Applicant's arguments filed *30 April 2009* have been fully considered but they are not persuasive.

The Applicant contends, "**Sotheran** does not teach 'wherein the rasterizing circuit rasterizes the first frame, if the controller does not provide the information regarding the second frame to the display engine before a first horizontal synchronization pulse following a vertical synchronization pulse associated with the second frame'" (see Page 5 of the Response filed *30 April 2009*). However, the examiner respectfully disagrees.

There is insufficient antecedent basis for "*the display engine*" limitation in the claims.

*Sotheran* explains, "The display address generator requests a new display buffer, once every vsync, via a two-wire interface. If there is a buffer flagged as READY, then that will be allocated to display by the buffer manager. If there is no READY buffer, the previously displayed buffer will be repeated" (see Column 296, Lines 17-21).

Therefore, *Sotheran* teaches not providing the information [e.g., *buffer not flagged as READY*] regarding the second frame to the display engine following a vertical synchronization pulse [e.g., *wherein vsync for the first frame and second frame are both "associated" -- in different ways -- with the second frame*].

*Sotheran* also goes on to define 'vdelay' as "*The number of hsync pulses following a vsync pulse before the first line of video or border... The minimum vdelay is zero. The first hsync is the first active line*" (see Column 333, Lines 48-59).

Therefore, *Sotheran* clearly teaches at least one first horizontal synchronization pulse [e.g., *hsync*] following a vertical synchronization pulse [e.g., *vsync*].

The Applicant contends, "*Sotheran* clearly does not teach or fairly suggest '*wherein the rasterizing circuit rasterizes the second frame, if the controller does provides the information regarding the second frame to the display engine after the vertical synchronization pulse associated with the second frame and before a first horizontal synchronization pulse following a vertical synchronization pulse associated with the second frame*'" (see Page 5 of the Response filed 30 April 2009). However, the examiner respectfully disagrees.

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In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., *the controller does provides the information regarding the second frame to the display engine*) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant's arguments with respect to claims 8, 9, 11-14, and 21 have been considered but are moot in view of the new ground(s) of rejection.

By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571)272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeff Piziali/  
Primary Examiner, Art Unit 2629  
14 July 2009